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- CLAIMS/Current Patent Legal Status (File 123)
- CLAIMS/U.S. Patents (File 340)
- Chinese Patent Abstracts in English (File 344)
- Derwent Patents Citation Index (File 342)
- Derwent World Patents Index (for users in Japan) (File 352)
- Derwent World Patents Index First View (File 331)
- Derwent World Patents Index (File 351)
- Derwent World Patents Index (File 350)
- Ei EnCompassPat (File 353)
- European Patents Fulltext (File 348)
- French Patents (File 371)
- German Patents Fulltext (File 324)
- IMS Patent Focus (File 447, 947)
- INPADOC/Family and Legal Status (File 345)
- JAPIO - Patent Abstracts of Japan (File 347)
- LitAlert (File 670)
- U.S. Patents Fulltext (1971-1975) (File 652)
- U.S. Patents Fulltext (1976-present) (File 654)
- WIPO/PCT Patents Fulltext (File 349)
- TRADEMARKSCAN - U.S. Federal (File 226)

DialogLink 5 Release Notes
New features available in the latest release of DialogLink 5 (August 2006)

- Ability to resize images for easier incorporation into DialogLink Reports
- New settings allow users to be prompted to save Dialog search sessions in the format of their choice (Microsoft Word, RTF, PDF, HTML, or TEXT)
- Ability to set up Dialog Alerts by Chemical Structures and the addition of Index Chemicus as a structure searchable database
- Support for connections to STN Germany and STN Japan services

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```
? Help Log On Msg
           *** ANNOUNCEMENTS ***
                    ***
*** FREE FILE OF THE MONTH (April) Promt and Trade &
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Database (Files 16 and 148)
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and trademark databases, a link to an online order form is displayed
in your search results, saving you time in obtaining the file
histories you need. See HELP FILEHIST for more information about
how to use the link and a list of files that contain the link.

NEW FILE
***File 651, TRADEMARKSCAN(R) - China. See HELP NEWS 651 for details.
RESUMED UPDATING
***File 523, D&B European Financial Records
***
RELOADS COMPLETED
***Files 154&155, MEDLINE(R)
***File 126, TRADEMARKSCAN(R) - United Kingdom
***File 228, TRADEMARKSCAN(R) - Spain
***File 672, TRADEMARKSCAN(R) - Germany
***File 655, TRADEMARKSCAN(R) - Korea
***File 656, TRADEMARKSCAN(R) - Australia
***File 657, TRADEMARKSCAN(R) - France
***File 673, TRADEMARKSCAN(R) - Italy
***
FILES RENAMED
***File 321, PLASPEC now known as Plastic Properties Database
***
FILES REMOVED
***File 301, CHEMNAME - please use File 398 ChemSearch
***File 388,PEDS: Defense Program Summaries
***File 588,DMS-FI Contract Awards

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```
 >>>http://www.dialog.com/whatsnew/.  You can find
news about   <<<
 >>>a specific database by entering HELP NEWS <file
number>.    <<<

? Help Off Line
* * *
Connecting to sahmed - Dialog - 291839
Connected to Dialog via SMS004043333

?  b
9,15,16,20,47,75,80,88,98,112,141,148,160,275,264,331
, 340, 350, 351,
352,369,370,484,553,570,608,620,613,621,623,624,634,6
35,636,647,696,674, 324, 344, 348, 349,
371,810,813,587
>>>W:          352 is unauthorized
1 of the specified files is not available
```

[File 9] **Business & Industry(R)** Jul/1994-2009/Apr 15
(c) 2009 Gale/Cengage. All rights reserved.

[File 15] **ABI/Inform(R)** 1971-2009/Apr 17
(c) 2009 ProQuest Info&Learning. All rights reserved.

[File 16] **Gale Group PROMT(R)** 1990-2009/Mar 26
(c) 2009 Gale/Cengage. All rights reserved.
**File 16: UD/banner does not reflect last processed date*

[File 20] **Dialog Global Reporter** 1997-2009/Apr 17
(c) 2009 Dialog. All rights reserved.

[File 47] **Gale Group Magazine DB(TM)** 1959-2009/Apr 08
(c) 2009 Gale/Cengage. All rights reserved.

[File 75] **TGG Management Contents(R)** 86-2009/Mar W2
(c) 2009 Gale/Cengage. All rights reserved.

[File 80] **TGG Aerospace/Def.Mkts(R)** 1982-2009/Mar 24
(c) 2009 Gale/Cengage. All rights reserved.

[File 88] **Gale Group Business A.R.T.S.** 1976-2009/Apr 16
(c) 2009 Gale/Cengage. All rights reserved.

[File 98] **General Sci Abs** 1984-2009/Apr
(c) 2009 The HW Wilson Co. All rights reserved.

[File 112] **UBM Industry News** 1998-2004/Jan 27
(c) 2004 United Business Media. All rights reserved.

File 112: This file is closed. For more recent UBM/CMP records, please search DIALOG Newsroom files.

[File 141] **READERS GUIDE** 1983-2009/MAR
(c) 2009 THE HW WILSON CO. All rights reserved.

[File 148] **Gale Group Trade & Industry DB** 1976-2009/Apr 02
(c) 2009 Gale/Cengage. All rights reserved.
File 148: The CURRENT feature is not working in File 148. See HELP NEWS148.

[File 160] **Gale Group PROMT(R)** 1972-1989
(c) 1999 The Gale Group. All rights reserved.

[File 275] **Gale Group Computer DB(TM)** 1983-2009/Mar 23
(c) 2009 Gale/Cengage. All rights reserved.

[File 264] **DIALOG Defense Newsletters** 1989-2009/Apr 17
(c) 2009 Dialog. All rights reserved.

[File 331] **Derwent WPI First View/UD=200919**
(c) 2009 Thomson Reuters. All rights reserved.
File 331: Due to update delays, First View updates 200910-200913 will be skipped to align update codes with WPI. There will be no data loss.

[File 340] **CLAIMS(R)/US Patent** 1950-09/Apr 14
(c) 2009 IFI/CLAIMS(R). All rights reserved.

[File 350] **Derwent WPIX** 1963-2009/UD=200920
(c) 2009 Thomson Reuters. All rights reserved.

[File 351] **Derwent WPI** 1963-2009/UD=200920
(c) 2009 Thomson Reuters. All rights reserved.

[File 369] **New Scientist** 1994-2009/Mar W5
(c) 2009 Reed Business Information Ltd. All rights reserved.

[File 370] **Science** 1996-1999/Jul W3
(c) 1999 AAAS. All rights reserved.
File 370: This file is closed (no updates). Use File 47 for more current information.

[File 484] **Periodical Abs Plustext** 1986-2009/Apr W2
(c) 2009 ProQuest. All rights reserved.
File 484: Despite the gap in UDs all content is present.

[File 553] **Wilson Bus. Abs.** 1982-2009/Apr
(c) 2009 The HW Wilson Co. All rights reserved.

[File 570] **Gale Group MARS(R)** 1984-2009/Mar 27
(c) 2009 Gale/Cengage. All rights reserved.

[File 608] **MCT Information Svc.** 1992-2009/Apr 17
(c) 2009 MCT Information Svc. All rights reserved.

[File 620] **EIU:Viewswire** 2009/Apr 16
(c) 2009 Economist Intelligence Unit. All rights reserved.

[File 613] **PR Newswire** 1999-2009/Apr 17
(c) 2009 PR Newswire Association Inc. All rights reserved.
**File 613: File 613 now contains data from 5/99 forward. Archive data (1987-4/99) is available in File 813.*

[File 621] **Gale Group New Prod.Annou.(R)** 1985-2009/Mar 13
(c) 2009 Gale/Cengage. All rights reserved.

[File 623] **Business Week** 1985-2009/Apr 15
(c) 2009 The McGraw-Hill Companies Inc. All rights reserved.

[File 624] **McGraw-Hill Publications** 1985-2009/Apr 17
(c) 2009 McGraw-Hill Co. Inc. All rights reserved.

[File 634] **San Jose Mercury** Jun 1985-2009/Apr 16
(c) 2009 San Jose Mercury News. All rights reserved.

[File 635] **Business Dateline(R)** 1985-2009/Apr 17
(c) 2009 ProQuest Info&Learning. All rights reserved.

[File 636] **Gale Group Newsletter DB(TM)** 1987-2009/Mar 27
(c) 2009 Gale/Cengage. All rights reserved.

[File 647] **UBM Computer Fulltext** 1988-2009/Feb W3
(c) 2009 UBM, LLC. All rights reserved.

[File 696] **DIALOG Telecom. Newsletters** 1995-2009/Apr 08
(c) 2009 Dialog. All rights reserved.

[File 674] **Computer News Fulltext** 1989-2006/Sep W1
(c) 2006 IDG Communications. All rights reserved.
**File 674: File 674 is closed (no longer updates).*

[File 324] **GERMAN PATENTS FULLTEXT** 1967-200916
(c) 2009 UNIVENTIO/THOMSON. All rights reserved.

[File 344] **Chinese Patents Abs** Jan 1985-2006/Jan
(c) 2006 European Patent Office. All rights reserved.

[File 348] **EUROPEAN PATENTS** 1978-200915
(c) 2009 European Patent Office. All rights reserved.

[File 349] **PCT FULLTEXT** 1979-2009/UB=20090402|UT=20090326
(c) 2009 WIPO/Thomson. All rights reserved.

[File 371] **French Patents** 1961-2002/BOPI 200209
(c) 2002 INPI. All rts. reserv. All rights reserved.

[File 810] **Business Wire** 1986-1999/Feb 28
(c) 1999 Business Wire . All rights reserved.

[File 813] **PR Newswire** 1987-1999/Apr 30
(c) 1999 PR Newswire Association Inc. All rights reserved.

[File 587] **Jane`s Defense&Aerospace** 2009/Mar W3
(c) 2009 Jane`s Information Group. All rights reserved.

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?  s au=(GULATI MANU or GULATI, MANU or GULATI M? or
GULATI, M?)
>>>W:  One or more prefixes are unsupported
  or undefined in one or more files.
            80   AU=GULATI MANU
            46   AU=GULATI, MANU
           108   AU=GULATI M?
            95   AU=GULATI, M?
S1         149   S AU=(GULATI MANU OR GULATI, MANU OR
GULATI M? OR GULATI, M?)

?  s au=(MOLL LAURENT  or MOLL, LAURENT  or MOLL L?
or MOLL, L?)
>>>W:  One or more prefixes are unsupported
  or undefined in one or more files.
            48   AU=MOLL LAURENT
            32   AU=MOLL, LAURENT
           203   AU=MOLL L?
           141   AU=MOLL, L?
S2         234   AU=(MOLL LAURENT  OR MOLL, LAURENT
OR MOLL L? OR MOLL, L?)

?
?  s s1 and s2 and SPI
           149   S1
           234   S2
         72290   SPI
S3          15   S S1 AND S2 AND SPI

?  S S3 not py>2003
Processing
Processing
Processing
Processing
Processing
Processing
Processing
           15   S3
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      84342997   PY>2003
S4           0   S S3 NOT PY>2003

?  TYPE S3/3,K/ALL
```

3/3,K/1 (Item 1 from file: 340) **Links**
Fulltext available through: Order File History

CLAIMS(R)/US Patent
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10643974
E/APPARATUS AND METHOD TO RECEIVE AND ALIGN INCOMING DATA IN A BUFFER TO EXPAND DATA WIDTH BY UTILIZING A SINGLE WRITE PORT MEMORY DEVICE

Inventors:**Gulati Manu** (US); **Moll Laurent R** (US)

Assignee: Unassigned Or Assigned To Individual
Assignee Code: 68000
Probable Assignee (A1): Broadcom Corp
Attorney, Agent or Firm: GARLICK HARRISON & MARKISON LLP, P.O. BOX
160727, AUSTIN, TX, 78716-0727, US

Publication	Application Number	Kind	Date	Number	Date
	US 20040151203 A1		20040805	US 2003685231	20031014
Cont.-in-part of:	Pending			US 2003356661	20030131
Priority Applic:				US 2003685231	20031014
				US 2003356661	20030131

Document Type:
Inventors:**Gulati Manu**...

...**Moll Laurent R**
Non-exemplary Claims:

...7. The apparatus of claim 4 wherein the received data is based on
SPI-4 protocol...

...14 wherein one input decode and routing unit decodes and

routes incoming
data based on **SPI**-4 protocol...

...20. The method of claim 19 wherein the data is based on **SPI**-4 protocol...

3/3,K/2 (Item 2 from file: 340) **Links**
Fulltext available through: Order File History
CLAIMS(R)/US Patent
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10512500 2004-0019704
E/MULTIPLE PROCESSOR INTEGRATED CIRCUIT HAVING CONFIGURABLE
PACKET-BASED INTERFACES
Inventors:**Gulati Manu** (US); Keller James (US); **Moll Laurent** (US); Sano Barton (US)
Assignee: Unassigned Or Assigned To Individual
Assignee Code: 68000
Attorney, Agent or Firm: GARLICK HARRISON & MARKISON LLP, P.O. BOX
160727, AUSTIN, TX, 78716-0727, US

Publication Number	Kind	Date	Application Number	Date
US 20040019704 A1		20040129	US 2003356390	20030131
Priority Applic:			US 2003356390	20030131
Provisional Applic:			US 60-380740	20020515
			US 60-419032	20021016

Document Type:
Inventors:**Gulati Manu**...

...**Moll Laurent**
Non-exemplary Claims:

...at least one of a HyperTransport (HT) input/output port and a System
Packet Interface (**SPI**) input/ output port; and the second configurable packet-based interface is configured to provide at least
one of the HyperTransport (HT) input/output port and the System Packet
Interface (**SPI**) input/ output port...

...packet-based protocol further comprises at least one of HyperTransport
(HT) and System Packet Interface (**SPI**).
...

...at least one of a HyperTransport (HT) input/output port and a System
Packet Interface (**SPI**) input/output port; and the second configurable packet-based interface is configured to provide at least
one of the HyperTransport (HT) input/output port and the System Packet
Interface (**SPI**) input/output port...

...at least one of a HyperTransport (HT) input/output port and a System
Packet Interface (**SPI**) input/output port; and the second packet-based interface is configured to provide at least one of the
HyperTransport (HT) input/output port and the System Packet Interface (
SPI) input/output port

3/3,K/3 (Item 3 from file: 340) **Links**
Fulltext available through: Order File History
CLAIMS(R)/US Patent
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10510609 2004-0017813
E/TRANSMITTING DATA FROM A PLURALITY OF VIRTUAL CHANNELS VIA A MULTIPLE PROCESSOR DEVICE
Inventors:**Gulati Manu** (US); Keller James (US); **Moll Laurent** (US)
Assignee: Unassigned Or Assigned To Individual
Assignee Code: 68000
Probable Assignee (A1): Broadcom Corp
Attorney, Agent or Firm: GARLICK HARRISON & MARKISON LLP, P.O. BOX
160727, AUSTIN, TX, 78716-0727, US

Publication	Application Number	Kind	Date	Number	Date
	US 20040017813	A1	20040129	US 2003356348	20030131
Priority Applic:				US 2003356348	20030131
Provisional Applic:				US 60-380740	20020515
				US 60-419040	20021016

Document Type:
Inventors:**Gulati Manu**...

...**Moll Laurent**

Abstract: ...the stored data in accordance with a 1st or 2nd transmission
protocol (e.g. , HT, **SPI**, et cetera) to produce a packetized transmission.
Non-exemplary Claims:

...to produce buffered data; packetizing the buffered data in accordance with a System Packet Interface (**SPI**) protocol to produce **SPI** packets; and elastic storing the **SPI** packets ...

...to produce buffered data; packetize the buffered data in accordance with

a System Packet Interface (**SPI**) protocol to produce **SPI** packets; and elastic store the **SPI** packets...

...to produce buffered data; packetize the buffered data in accordance with
a System Packet Interface (**SPI**) protocol to produce **SPI** packets; and elastic store the **SPI** packets.

3/3,K/4 (Item 4 from file: 340) **Links**
Fulltext available through: Order File History
CLAIMS(R)/US Patent
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04936326
E/(A1) HYPERTRANSPORT/**SPI**-4 INTERFACE SUPPORTING
CONFIGURABLE DESKEWING
(B2) HYPERTRANSPORT/**SPI**-4 INTERFACE SUPPORTING CONFIGURABLE
DESKEWING
Inventors:**Gulati Manu** (US); **Moll Laurent R** (US)

Assignee: (A1) Unassigned Or Assigned To Individual
(B2) Broadcom Corp
Assignee Code: (A1) 68000; (B2) 59773
Probable Assignee (A1): Broadcom Corp
Attorney, Agent or Firm: Garlick Harrison & Markison; Garlick,
Bruce E.
; Smith, Kevin L.

Publication Number	Kind	Application Date	Number	Date
US 20040130347	A1	20040708	US 2003742060	20031220
US 7490187	B2	20090210	US 2003742060	20031220

Cont.-in-part of: Pending US 2003356390
20030131
Prior Publication: US 20040130347 A1 20040708
Priority Applic: US 2003742060
20031220
US 2003356390
20030131
Provisional Applic: US 60-380740
20020515
US 60-419032
20021016
Calculated Expiration: 20230131
Notes: Subject to any Disclaimer, the term of this patent is
extended or
adjusted under 35 USC 154(b) by 940 days.

...HYPERTRANSPORT/**SPI**-4 INTERFACE SUPPORTING CONFIGURABLE
DESKEWING
...

...HYPERTRANSPORT/**SPI**-4 INTERFACE SUPPORTING CONFIGURABLE DESKEWING
Document Type:
Inventors:**Gulati Manu...**

...**Moll Laurent R**
Non-exemplary Claims:

...digital interface of claim 1, wherein the at least one other interface standard includes the **SPI**-4 Standard...

...The method of claim 11, wherein the at least one other interface standard includes the **SPI**-4 Standard...

...digital interface of claim 1, wherein the at least one other interface standard includes the **SPI**-4 Standard...

...The method of claim 11, wherein the at least one other interface standard includes the **SPI**-4 Standard...

3/3,K/5 (Item 5 from file: 340) **Links**
Fulltext available through: Order File History
CLAIMS(R)/US Patent
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04735596
E/(A1) APPARATUS AND METHOD TO RECEIVE AND DECODE INCOMING DATA AND TO HANDLE REPEATED SIMULTANEOUS SMALL FRAGMENTS
(B2) APPARATUS AND METHOD TO RECEIVE AND DECODE INCOMING DATA AND TO HANDLE REPEATED SIMULTANEOUS SMALL FRAGMENTS
Inventors:**Gulati Manu** (US); **Moll Laurent R** (US)

Assignee: (A1) Unassigned Or Assigned To Individual
(B2) Broadcom Corp
Assignee Code: (A1) 68000; (B2) 59773
Probable Assignee (A1): Broadcom Corp
Attorney, Agent or Firm: Garlick Harrison & Markison

Publication Number	Kind	Application Date	Number	Date
US 20040153586	A1	20040805	US 2003684998	20031014
US 7319702	B2	20080115	US 2003684998	20031014

Cont.-in-part of: Pending US 2003356661 20030131
Prior Publication: US 20040153586 A1 20040805
Priority Applic: US 2003684998 20031014
US 2003356661 20030131
Calculated Expiration: 20230131
Notes: Subject to any Disclaimer, the term of this patent is extended or
adjusted under 35 USC 154(b) by 996 days.

Document Type:
Inventors:**Gulati Manu**...

...**Moll Laurent R**
Non-exemplary Claims:

...apparatus of claim 6, wherein the data aligner to receive data is

based on the **SPI**-4 protocol...

...apparatus of claim 12, wherein the data aligner to receive data is based on the **SPI**-4 protocol...

...circuit of claim 17, wherein the data aligner to receive data is based on the **SPI**-4 protocol...

...The method of claim 19, wherein the segmenting the data stream segments data based on **SPI**-4 protocol...

...apparatus of claim 6, wherein the data aligner to receive data is based on the **SPI**-4 protocol...

...apparatus of claim 12, wherein the data aligner to receive data is based on the **SPI**-4 protocol...

...circuit of claim 17, wherein the data aligner to receive data is based on the **SPI**-4 protocol...

...The method of claim 19, wherein the segmenting the data stream segments data based on **SPI**-4 protocol.

3/3,K/6 (Item 6 from file: 340) **Links**
Fulltext available through: Order File History
CLAIMS(R)/US Patent
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04722750
E/(A1) TRANSPARENT DATA FORMAT WITHIN HOST DEVICE SUPPORTING DIFFERING TRANSACTION TYPES
(B2) TRANSPARENT DATA FORMAT WITHIN HOST DEVICE SUPPORTING DIFFERING TRANSACTION TYPES
Inventors:**Gulati Manu** (US); **Moll Laurent R** (US);
Rowlands Joseph B (US)
Assignee: (A1) Unassigned Or Assigned To Individual
(B2) Broadcom Corp
Assignee Code: (A1) 68000; (B2) 59773
Probable Assignee (A1): Broadcom Corp
Attorney, Agent or Firm: Garlick Harrison & Markison; Garlick, Bruce E.

Publication Number	Kind	Date	Application Number	Date
US 20040151175	A1	20040805	US 2003684989	20031014
US 7313146	B2	20071225	US 2003684989	20031014

Cont.-in-part of: Pending US 2003356661 20030131
Prior Publication: US 20040151175 A1 20040805
Priority Applic: US 2003684989 20031014
US 2003356661 20030131
Calculated Expiration: 20230131
Notes: Subject to any Disclaimer, the term of this patent is extended or
adjusted under 35 USC 154(b) by 996 days.

Document Type:
Inventors:**Gulati Manu**...

...**Moll Laurent R**
Non-exemplary Claims:

...4. The system of claim 3, wherein: the packet based interface

is a
SPI-4 interface; and the address based interface is one of a HyperTransport interface, a PCI...

...21. The method of claim 20, wherein: the packet-based interface is a
SPI-4 interface; and the input/output-based interface is one of a
HyperTransport interface, a...

...4. The system of claim 3, wherein: the packet based interface is a
SPI-4 interface; and the address based interface is one of a HyperTransport interface, a PCI...
...21. The method of claim 20, wherein: the packet-based interface is a
SPI-4 interface; and the input/output-based interface is one of a
HyperTransport interface, a...

3/3,K/7 (Item 7 from file: 340) **Links**
Fulltext available through: Order File History
CLAIMS(R)/US Patent
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04292563
E/(A1) SYSTEM HAVING INTERFACES AND SWITCH THAT SEPARATES
COHERENT AND PACKET TRAFFIC
(B2) SYSTEM HAVING INTERFACES AND SWITCH THAT SEPARATES
COHERENT AND
PACKET TRAFFIC
Inventors:**Gulati Manu** (US); Keller James B (US); **Moll Laurent R** (US); Oner Koray (US); Rowlands Joseph B (US); Sano Barton J (US)
Assignee: (A1) Unassigned Or Assigned To Individual
(B2) Broadcom Corp
Assignee Code: (A1) 68000; (B2) 59773
Attorney, Agent or Firm: Garlick Harrison & Markison

Publication Number	Kind	Publication Date	Application Number	Application Date
US 20040221072	A1	20041104	US 2004861624	20040604
US 6941406	B2	20050906	US 2004861624	20040604

Continuation of: US 6748479 US 2002270029 20021011
Prior Publication: US 20040221072 A1 20041104
Priority Applic: US 2004861624 20040604
US 2002270029 20021011
Provisional Applic: US 60-331789 20011120
US 60-344713 20011224
US 60-348717 20020114
US 60-348777 20020114
US 60-380740 20020515
Calculated Expiration: 20221011
Notes: Subject to any Disclaimer, the term of this patent is extended or
adjusted under 35 USC 154(b) by 2 days.. This Patent is subject to a

Terminal Disclaimer.

Document Type:
Inventors:**Gulati Manu**...

...**Moll Laurent R**
Non-exemplary Claims:

...The apparatus of claim 1 wherein the interface is compatible as a
system packet interface (**SPI**).
...

...apparatus of claim 1 wherein the interface is compatible as a system
packet interface-4 (**SPI**-4...

...HT) interface and at least one interface circuit is compatible as a
system packet interface (**SPI**).
...

...HT) interface and at least one interface circuit is compatible as a
system packet interface (**SPI**).
...

...HT) interface and at least one interface circuit is compatible as a
system packet interface (**SPI**).

3/3,K/8 (Item 1 from file: 350) **Links**
Fulltext available through: Order File History
Derwent WPIX
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0014363146 *Drawing available*
WPI Acc no: 2004-551820/200453
Related WPI Acc No: 2003-443150; 2003-443151; 2003-459993; 2003-471483; 2003-902176; 2004-070464; 2004-168050; 2004-179407; 2004-179709; 2004-190759; 2004-202696; 2004-225234; 2004-246804; 2004-247141; 2004-340077; 2004-347568; 2004-603213; 2004-614150; 2004-624116; 2004-624314; 2005-010789; 2005-010807; 2005-712402; 2005-785089; 2006-796373; 2007-717114; 2003-459995; 2003-485085; 2003-485086; 2003-485087; 2003-660330; 2003-661006; 2003-846837; 2003-846838; 2003-856022; 2003-880127; 2003-880128; 2003-880129; 2004-033251; 2004-033256; 2007-205863
XRPX Acc No: N2004-436504
Hypertransport interface for data communication, has enablement control module that disables and enables deskew blocks and deskew module when they support hyper transport standard and other interface standard, respectively
Patent Assignee: GULATI M (GULA-I); MOLL L R (MOLL-I); BROADCOM CORP (BROA-N)
Inventor: **GULATI M**; **MOLL L R**

Patent Family (2 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 20040130347	A1	20040708	US 2002380740	P	20020515	200453	B
			US 2002419032	P	20021016		
			US 2003356390	A	20030131		
			US 2003742060	A	20031220		
US 7490187	B2	20090210	US 2002380740	P	20020515	200917	E
			US 2002419032	P	20021016		
			US 2003356390	A	20030131		
			US 2003742060	A	20031220		

Priority Applications (no., kind, date): US 2002380740 P 20020515; US 2002380740 P 20020515; US 2002419032 P 20021016; US 2002419032 P 20021016; US 2003356390 A 20030131; US 2003742060 A 20031220

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
US 20040130347	A1	EN	28	15	Related to Provisional	US 2002380740
					Related to Provisional	US 2002419032
					C-I-P of application	US 2003356390
US 7490187	B2	EN			Related to Provisional	US 2002380740
					Related to Provisional	US 2002419032
					C-I-P of application	US 2003356390

Original Titles: Hypertransport/**SPI**-4 interface supporting configurable deskewing... ...Hypertransport/**SPI**-4 interface supporting configurable deskewing Inventor: **GULATI M**... ...**MOLL L R** Original Publication Data by AuthorityArgentina**Publication No.** Inventor name & address:**Moll, Laurent R**... ...**Gulati, Manu**... ...**Gulati, Manu**... ...**Moll, Laurent R**

3/3,K/9 (Item 2 from file: 350) **Links**
Fulltext available through: Order File History
Derwent WPIX
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0013987003 *Drawing available*
WPI Acc no: 2004-168050/200416
Related WPI Acc No: 2003-443150; 2003-443151; 2003-459993; 2003-471483; 2003-880128; 2003-902176; 2004-033256; 2004-070464; 2004-179407; 2004-179709; 2004-190759; 2004-202696; 2004-225234; 2004-246804; 2004-247141; 2004-340077; 2004-347568; 2004-551820; 2004-603213; 2004-614150; 2004-624116; 2004-624314; 2004-718057; 2004-736067; 2005-010789; 2005-010807; 2005-712402; 2005-785089; 2006-796373; 2007-717114
XRPX Acc No: N2004-134026
Virtual channel data transmitting method for data communications, involves packetizing stored data based on transmission protocols when respective protocol is indicated during cycle different from other two cycles
Patent Assignee: GULATI M (GULA-I); KELLER J (KELL-I); MOLL L (MOLL-I)
Inventor: **GULATI M**; KELLER J; **MOLL L**

Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 20040017813	A1	20040129	US 2002380740	P	20020515	200416	B
			US 2002419040	P	20021016		
			US 2003356348	A	20030131		

Priority Applications (no., kind, date): US 2002380740 P 20020515; US 2002419040 P 20021016; US 2003356348 A 20030131

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
US 20040017813	A1	EN	20	9	Related to Provisional	US 2002380740
					Related to Provisional	US 2002419040

Inventor: **GULATI M**... ...**MOLL L** Original Publication Data by AuthorityArgentina**Publication No.** Inventor name & address:**Gulati, Manu**... ...**Moll, Laurent** ...**Original Abstracts:**the stored data in accordance with a 1st or 2nd transmission protocol (e.g., HT, **SPI**, et cetera) to produce a packetized transmission.

3/3,K/10 (Item 1 from file: 351) **Links**
Fulltext available through: Order File History
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0014363146 *Drawing available*
WPI Acc no: 2004-551820/200453
Related WPI Acc No: 2003-443150; 2003-443151; 2003-459993; 2003-471483; 2003-902176; 2004-070464; 2004-168050; 2004-179407; 2004-179709; 2004-190759; 2004-202696; 2004-225234; 2004-246804; 2004-247141; 2004-340077; 2004-347568; 2004-603213; 2004-614150; 2004-624116; 2004-624314; 2005-010789; 2005-010807; 2005-712402; 2005-785089; 2006-796373; 2007-717114; 2003-459995; 2003-485085; 2003-485086; 2003-485087; 2003-660330; 2003-661006; 2003-846837; 2003-846838; 2003-856022; 2003-880127; 2003-880128; 2003-880129; 2004-033251; 2004-033256; 2007-205863
XRPX Acc No: N2004-436504
Hypertransport interface for data communication, has enablement control module that disables and enables deskew blocks and deskew module when they support hyper transport standard and other interface standard, respectively
Patent Assignee: GULATI M (GULA-I); MOLL L R (MOLL-I); BROADCOM CORP (BROA-N)
Inventor: **GULATI M**; **MOLL L R**

Patent Family (2 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 20040130347	A1	20040708	US 2002380740	P	20020515	200453	B
			US 2002419032	P	20021016		
			US 2003356390	A	20030131		
			US 2003742060	A	20031220		
US 7490187	B2	20090210	US 2002380740	P	20020515	200917	E
			US 2002419032	P	20021016		
			US 2003356390	A	20030131		
			US 2003742060	A	20031220		

Priority Applications (no., kind, date): US 2002380740 P 20020515; US 2002380740 P 20020515; US 2002419032 P 20021016; US 2002419032 P 20021016; US 2003356390 A 20030131; US 2003742060 A 20031220

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
US 20040130347	A1	EN	28	15	Related to Provisional	US 2002380740
					Related to Provisional	US 2002419032
					C-I-P of application	US 2003356390
US 7490187	B2	EN			Related to Provisional	US 2002380740
					Related to Provisional	US 2002419032
					C-I-P of application	US 2003356390

Original Titles: Hypertransport/**SPI**-4 interface supporting configurable deskewing... ...Hypertransport/**SPI**-4 interface supporting configurable deskewing Inventor: **GULATI M**... ...**MOLL L R** Original Publication Data by AuthorityArgentina**Publication No.** Inventor name & address:**Moll, Laurent R**... ...**Gulati, Manu**... ...**Gulati, Manu**... ...**Moll, Laurent R**

3/3,K/11 (Item 2 from file: 351) **Links**
Fulltext available through: Order File History
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0013987003 *Drawing available*
WPI Acc no: 2004-168050/200416
Related WPI Acc No: 2003-443150; 2003-443151; 2003-459993; 2003-471483; 2003-880128; 2003-902176; 2004-033256; 2004-070464; 2004-179407; 2004-179709; 2004-190759; 2004-202696; 2004-225234; 2004-246804; 2004-247141; 2004-340077; 2004-347568; 2004-551820; 2004-603213; 2004-614150; 2004-624116; 2004-624314; 2004-718057; 2004-736067; 2005-010789; 2005-010807; 2005-712402; 2005-785089; 2006-796373; 2007-717114
XRPX Acc No: N2004-134026
Virtual channel data transmitting method for data communications, involves packetizing stored data based on transmission protocols when respective protocol is indicated during cycle different from other two cycles
Patent Assignee: GULATI M (GULA-I); KELLER J (KELL-I); MOLL L (MOLL-I)
Inventor: **GULATI M**; KELLER J; **MOLL L**

Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 20040017813	A1	20040129	US 2002380740	P	20020515	200416	B
			US 2002419040	P	20021016		
			US 2003356348	A	20030131		

Priority Applications (no., kind, date): US 2002380740 P 20020515; US 2002419040 P 20021016; US 2003356348 A 20030131

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
US 20040017813	A1	EN	20	9	Related to Provisional	US 2002380740
					Related to Provisional	US 2002419040

Inventor: **GULATI M**... ...**MOLL L** Original Publication Data by AuthorityArgentina**Publication No.** Inventor name & address:**Gulati, Manu**... ...**Moll, Laurent** ...**Original Abstracts:**the stored data in accordance with a 1st or 2nd transmission protocol (e.g., HT, **SPI**, et cetera) to produce a packetized transmission.

3/3K/12 (Item 1 from file: 348) **Links**
Fulltext available through: Order File History
EUROPEAN PATENTS
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01581453
System having two or more packet interfaces, a switch, a shared packet DMA (Direct Memory Access) circuit and a L2 (Level 2) cache
System, welches zwei oder mehr Paketschnittstellen, einen Schalter, einen gemeinsamen Paket-DMA (Direct Memory Access)-Schaltkreis sowie einen L2 (Level 2) Cache aufweist
Systeme incluant deux ou plusieures interfaces de paquets, un commutateur, un circuit DMA (Direct Memory Access) de memoire partagee et une antememoire de second niveau

Patent Assignee:

- **Broadcom Corporation**; (2064671)
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  (Proprietor designated states: all)

Inventor:

- **Sano, Barton J.**
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  1211 Rosseau Drive; Sunnyvale, CA 94087; (US)
- **Gulati, Manu**
  1575 Vista Club Circle, Apartment 302; Santa Clara, CA 95054; (US)
- **...US)**
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- **Moll, Laurent R... ...US)**
  ; ;
- **Gulati, Manu...**
  ; ;

Legal Representative:

- **Jehle, Volker Armin (95141)**
  Patentanwalte Bosch, Graf von Stosch, Jehle, Fluggenstrasse 13; 80639 Munchen; (DE)

	Country	Number	Kind	Date	
Patent	EP	1313273	A1	20030521	(Basic)
	EP	1313273	B1	20051109	
Application	EP	2002025690		20021120	
Priorities	US	380740	P	20020515	
	US	331789	P	20011120	
	US	344713	P	20011224	

	US	348777	P	20020114	
	US	348717	P	20020114	
	US	269666		20021011	

Designated States:
AT; BE; BG; CH; CY; CZ; DE; DK; EE; ES;
FI; FR; GB; GR; IE; IT; LI; LU; MC; NL;
PT; SE; SK; TR;

Extended Designated States:
AL; LT; LV; MK; RO; SI;

International Patent Class (V7): H04L-012/56**Abstract Word Count:** 137
NOTE: 1
NOTE: Figure number on first page: 1

Type	Pub. Date	Kind	Text

Publication: English
Procedural: English
Application:English

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200321	944
SPEC A	(English)	200321	10940
CLAIMS B	(English)	200545	1078
CLAIMS B	(German)	200545	989
CLAIMS B	(French)	200545	1347
SPEC B	(English)	200545	10934
Total Word Count (Document A) 11885			
Total Word Count (Document B) 14348			
Total Word Count (All Documents) 26233			

Specification: ...carry packet data. For example, in some embodiments, the interfaces may be system packet interfaces (**SPI**) according to any level of the **SPI** specification set forth by the Optical Internetworking Forum (e.g. level 3, level 4, or level 5). In one particular embodiment, the interfaces may be **SPI**-4 phase 2 interfaces. In other embodiments, the interfaces may be HyperTransport(TM) (HT) interfaces ... ...illustrated embodiment, each interface circuit 20A-20C may be configurable to communicate on either the **SPI**-4 interface or the HT interface. Each interface circuit 20A-20C may be individually programmable, permitting various combinations of the HT and **SPI** -4 interfaces as interfaces 30A-30C. The programming may be performed in any fashion (e...defined by the interface from which the Rx circuit receives packet data. For example, the **SPI**-4 interface and the HT interface may both support 16 virtual channels in hardware (although more may be used by software in the **SPI**-4 interface, since an 8 bit virtual channel value is supported). Thus, each Rx circuit... ...embodiment of Fig. 3, the Rx circuit 26A includes a decoder 50 (which includes a **SPI** decoder 52 and an HT decoder 54 including a PoHT BAR1 register 56), the H... ...receives the input data from the interface 30A and decodes the data according to the **SPI** specification (in the **SPI** decoder 52) or the HT specification (in the HT decoder 54). One of the decoders ...circuit 26A-26C that received the packet. In particular, if the Rx circuit is receiving **SPI**-4 phase 2 traffic, the LE bit may indicate, when set, that a DIP-4 error occurred. The SE bit

may indicate, when set, that a **SPI**-4 abort control word was received in the packet or an error was detected in... ...field stores the IVC for a received packet, if the packet was transmitted on the **SPI** interface. For output queue descriptors, the VC field may store a value for which the... ...28C may append the bits to the OVC to generate the VC field in the **SPI**-4 packet. The memory buffer address field stores the address of the memory buffer indicated... ...of the system 10. Illustrated in Fig. 12 is exemplary packet data transmitted on a **SPI**-4 interface and the packet data stored in a set of input queues of the... ...to the packet DMA circuit 16 for storage in the memory 24. Transmitters on a **SPI**-4 interface (e.g. the Tx circuits 28A-28C) are permitted to segment the packets... ...packet fragments of different packets. For example, packets traveling in different virtual channels on the **SPI**-4 interface may have fragments interleaved on the **SPI**-4 interface. Illustrated on the **SPI**-4 interface in Fig. 12 is a first packet (P0) comprising packet fragments P01)), P02...

Specification: ...carry packet data. For example, in some embodiments, the interfaces may be system packet interfaces (**SPI**) according to any level of the **SPI** specification set forth by the Optical Internetworking Forum (e.g. level 3, level 4, or level 5). In one particular embodiment, the interfaces may be **SPI**-4 phase 2 interfaces. In other embodiments, the interfaces may be HyperTransport(TM) (HT) interfaces ... ...illustrated embodiment, each interface circuit 20A-20C may be configurable to communicate on either the **SPI**-4 interface or the HT interface. Each interface circuit 20A-20C may be individually programmable, permitting various combinations of the HT and **SPI** -4 interfaces as interfaces 30A-30C. The programming may be performed in any fashion (e... ...defined by the interface from which the Rx circuit receives packet data. For example, the **SPI**-4 interface and the HT interface may both support 16 virtual channels in hardware (although more may be used by software in the **SPI**-4 interface, since an 8 bit virtual channel value is supported). Thus, each Rx circuit...embodiment of Fig. 3, the Rx circuit 26A includes a decoder 50 (which includes a **SPI** decoder 52 and an HT decoder 54 including a PoHT BAR1 register 56), the H... ...receives the input data from the interface 30A and decodes the data according to the **SPI** specification (in the **SPI** decoder 52) or the HT specification (in the HT decoder 54). One of the decoders ... ...circuit 26A-26C that received the packet. In particular, if the Rx circuit is receiving **SPI**-4 phase 2 traffic, the LE bit may indicate, when set, that a DIP-4 error occurred. The SE bit may indicate, when set, that a **SPI**-4 abort control word was received in the packet or an error was detected in... ...field stores the IVC for a received packet, if the packet was transmitted on the **SPI** interface. For output queue descriptors, the VC field may store a value for which the... ...28C may append the bits to the OVC to generate the VC field in the **SPI**-4 packet. The memory buffer address field stores the address of the memory buffer indicated...of the system 10. Illustrated in Fig. 12 is exemplary packet data transmitted on a **SPI**-4 interface and the packet data stored in a set of input queues of the... ...to the packet DMA circuit 16 for storage in the memory 24. Transmitters on a **SPI**-4 interface (e.g. the Tx circuits 28A-28C) are permitted to segment the packets... ...packet fragments of different packets. For example, packets traveling in different virtual channels on the **SPI**-4 interface may have fragments interleaved on the **SPI**-4 interface. Illustrated on the **SPI**-4 interface in Fig. 12 is a first packet (P0) comprising packet fragments P01)), P02...

Claims: ...4, caracterise en ce que l'une des au moins deux interfaces est une interface **SPI** (<< System Packet Interfaces >>)

7. Le dispositif selon l'une quelconque des revendications 1 a 6...

3/3K/13 (Item 2 from file: 348) **Links**
Fulltext available through: Order File History
EUROPEAN PATENTS
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01581452
Systems including packet interfaces, and packet-DMA (Direct Memory Access) circuits for splitting and merging packet streams
Systeme, welche Paketschnittstellen und Paket-DMA (Direct Memory Access) Schaltkreise beinhalten, um Paketstrome zu teilen und zusammenzusetzen
Systemes incluant des interfaces de paquets et des circuits paquet-DMA (Direct Memory Access) pour separer et fusionner des flux de paquets

Patent Assignee:

- **Broadcom Corporation**; (2064671)
  16215 Alton Parkway; Irvine, California 92618; (US)
  (Proprietor designated states: all)

Inventor:

- **Sano, Barton**
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- **Gulati, Manu**
  1575 Vista Club Circle, Apt. 302; Santa Clara, CA 95054; (US)
- **...US)**
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- **Moll, Laurent R... ...US)**
  ; ;
- **Gulati, Manu...**
  ; ;

Legal Representative:

- **Jehle, Volker Armin, Dipl.-Ing. (95141)**
  Patentanwalte Bosch, Graf von Stosch, Jehle, Fluggenstrasse 13; 80639 Munchen; (DE)

	Country	Number	Kind	Date	
Patent	EP	1313272	A1	20030521	(Basic)
	EP	1313272	B1	20050323	
Application	EP	2002025688		20021120	
Priorities	US	331789	P	20011120	
	US	344713	P	20011224	
	US	348777	P	20020114	
	US	348717	P	20020114	
	US	380740	P	20020515	

	US	270016	20021011	

Designated States:
AT; BE; BG; CH; CY; CZ; DE; DK; EE; ES;
FI; FR; GB; GR; IE; IT; LI; LU; MC; NL;
PT; SE; SK; TR;

Extended Designated States:
AL; LT; LV; MK; RO; SI;

International Patent Class (V7): H04L-012/56**Abstract Word Count:** 90
NOTE: 1
NOTE: Figure number on first page: 1

Type	Pub. Date	Kind	Text

Publication: English
Procedural: English
Application:English

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200321	1562
SPEC A	(English)	200321	10969
CLAIMS B	(English)	200512	1342
CLAIMS B	(German)	200512	1319
CLAIMS B	(French)	200512	1496
SPEC B	(English)	200512	10298
Total Word Count (Document A) 12533			
Total Word Count (Document B) 14455			
Total Word Count (All Documents) 26988			

Specification: ...carry packet data. For example, in some embodiments, the interfaces may be system packet interfaces (**SPI**) according to any level of the **SPI** specification set forth by the Optical Internetworking Forum (e.g. level 3, level 4, or level 5). In one particular embodiment, the interfaces may be **SPI**-4 phase 2 interfaces. In other embodiments, the interfaces may be HyperTransport(TM) (HT) interfaces ... ...illustrated embodiment, each interface circuit 20A-20C may be configurable to communicate on either the **SPI**-4 interface or the HT interface. Each interface circuit 20A-20C may be individually programmable, permitting various combinations of the HT and **SPI** -4 interfaces as interfaces 30A-30C. The programming may be performed in any fashion (e... ...defined by the interface from which the Rx circuit receives packet data. For example, the **SPI**-4 interface and the HT interface may both support 16 virtual channels in hardware (although more may be used by software in the **SPI**-4 interface, since an 8 bit virtual channel value is supported). Thus, each Rx circuit... ...packet destination device (that is, a device that only sinks packets). In embodiments employing the **SPI**-4 interface, one **SPI**-4 link in the desired direction from an interface circuit 20A-20C may be used... ...circuit 26A may be used to receive packets from the packet source device via the **SPI**-4 interface. The Tx circuit 28A may be coupled via the **SPI**-4 interface to some other device, or may not be used. Similarly, if a packet... ...circuit 28A may be used to transmit packets to the packet destination device via the **SPI**-4 interface. The Rx circuit 26A may be coupled via the **SPI**-4 interface to some other device, or may not be used. Furthermore, in some embodiments, a packet source/destination device may be coupled to one **SPI**-4 link in one direction to one system 10 (e.g. from the device to the system 10) and

to another **SPI**-4 link in the other direction from another system 10 (e.g. from the system...embodiment of Fig. 5, the Rx circuit 26A includes a decoder 50 (which includes a **SPI** decoder 52 and an HT decoder 54 including a PoHT BAR1 register 56), the H... ...receives the input data from the interface 30A and decodes the data according to the **SPI** specification (in the **SPI** decoder 52) or the HT specification (in the HT decoder 54). One of the decoders ...

Specification: ...carry packet data. For example, in some embodiments, the interfaces may be system packet interfaces (**SPI**) according to any level of the **SPI** specification set forth by the Optical Internetworking Forum (e.g. level 3, level 4, or level 5). In one particular embodiment, the interfaces may be **SPI**-4 phase 2 interfaces. In other embodiments, the interfaces may be HyperTransport(TM) (HT) interfaces ... ...illustrated embodiment, each interface circuit 20A-20C may be configurable to communicate on either the **SPI**-4 interface or the HT interface. Each interface circuit 20A-20C may be individually programmable, permitting various combinations of the HT and **SPI** -4 interfaces as interfaces 30A-30C. The programming may be performed in any fashion (e... ...defined by the interface from which the Rx circuit receives packet data. For example, the **SPI**-4 interface and the HT interface may both support 16 virtual channels in hardware (although more may be used by software in the **SPI**-4 interface, since an 8 bit virtual channel value is supported). Thus, each Rx circuit...packet destination device (that is, a device that only sinks packets). In embodiments employing the **SPI**-4 interface, one **SPI**-4 link in the desired direction from an interface circuit 20A-20C may be used... ...circuit 26A may be used to receive packets from the packet source device via the **SPI**-4 interface. The Tx circuit 28A may be coupled via the **SPI**-4 interface to some other device, or may not be used. Similarly, if a packet... ...circuit 28A may be used to transmit packets to the packet destination device via the **SPI**-4 interface. The Rx circuit 26A may be coupled via the **SPI**-4 interface to some other device, or may not be used. Furthermore, in some embodiments, a packet source/destination device may be coupled to one **SPI**-4 link in one direction to one system 10 (e.g. from the device to the system 10) and to another **SPI**-4 link in the other direction from another system 10 (e.g. from the system... ...embodiment of Fig. 5, the Rx circuit 26A includes a decoder 50 (which includes a **SPI** decoder 52 and an HT decoder 54 including a PoHT BAR1 register 56), the H... ...receives the input data from the interface 30A and decodes the data according to the **SPI** specification (in the **SPI** decoder 52) or the HT specification (in the HT decoder 54). One of the decoders ...

3/3K/14 (Item 3 from file: 348) **Links**
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01581450

Systems using mix of packet, coherent, and noncoherent traffic to optimize transmission between systems

Systeme, welche eine Mischung aus paketartigem, koharentem und nicht-koharentem Verkehr verwenden, um die Ubertragung zwischen Systemen zu optimieren

Systemes utilisant un traffic mixte de paquets, traffic coherent et non-coherent pour l'optimisation de transmission entre systemes

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- **Sano, Barton, J.**
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- **...US)**
  ; ;
- **Moll, Laurent, R... ...US)**
  ; ;
- **Gulati, Manu...**
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Legal Representative:

- **Jehle, Volker Armin, Dipl.-Ing. (95141)**
  Patentanwalte Bosch, Graf von Stosch, Jehle, Fluggenstrasse 13; 80639 Munchen; (DE)

	Country	Number	Kind	Date	
Patent	EP	1313024	A1	20030521	(Basic)
	EP	1313024	B1	20041020	
Application	EP	2002025686		20021120	
Priorities	US	380740	P	20020515	
	US	331789	P	20011120	
	US	344713	P	20011224	

	US	348777	P	20020114	
	US	348717	P	20020114	
	US	269922		20021011	

Designated States:
AT; BE; BG; CH; CY; CZ; DE; DK; EE; ES;
FI; FR; GB; GR; IE; IT; LI; LU; MC; NL;
PT; SE; SK; TR;

Extended Designated States:
AL; LT; LV; MK; RO; SI;

International Patent Class (V7): G06F-013/14**Abstract Word Count:** 119
NOTE: 1
NOTE: Figure number on first page: 1

Type	Pub. Date	Kind	Text

Publication: English
Procedural: English
Application:English

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200321	1554
SPEC A	(English)	200321	20371
CLAIMS B	(English)	200443	1819
CLAIMS B	(German)	200443	1743
CLAIMS B	(French)	200443	2068
SPEC B	(English)	200443	20305
Total Word Count (Document A) 21928			
Total Word Count (Document B) 25935			
Total Word Count (All Documents) 47863			

Specification: ...interfaces using the PoHT extension. Alternative, such interfaces 30A-30C may be system packet interfaces (**SPI**) according to any level of the **SPI** specification set forth by the Optical Internetworking Forum (e.g. level 3, level 4, or level 5). In one particular embodiment, the interfaces may be **SPI**-4 phase 2 interfaces. In the illustrated embodiment, each interface circuit 20A-20C may be configurable to communicate on either the **SPI**-4 interface or the HT interface. Each interface circuit 20A-20C may be individually programmable, permitting various combinations of the HT and **SPI**-4 interfaces as interfaces 30A-30C. The programming may be performed in any fashion (e... ...g. transmitting the packet data as a payload of a command, such as PoHT). The **SPI**-4 interface may define 16 hardware virtual channels, extendable to 256 virtual channels in software... ...example, the interface 306 may be a HT interface (using the PoHT extension) or the **SPI**-4 interface, as desired. As used herein, a packet circuit includes any circuit which sources... ...example, the packet circuit 302 may be a media access control (MAC) circuit having a **SPI**-4 or HT packet interface. The packet circuit 302 may further comprise switches, routers, gateways...on the interface 308. In another embodiment, if desired, the interface 308 may be a **SPI**-4 interface if internode coherency is not used in the packet processing system 300.

The... ...defined by the interface from which the Rx circuit receives packet data. For example, the **SPI**-4 interface and the HT interface may both support 16 virtual channels in hardware

(although more may be used by software in the **SPI**-4 interface, since an 8 bit virtual channel value is supported). Thus, each Rx circuit... ...embodiment of Fig. 8, the Rx circuit 26A includes a decoder 60 (which includes a **SPI** decoder 62 and an HT decoder 64 including a PoHT BAR1 register 66), a hash... ...receives the input data from the interface 30A and decodes the data according to the **SPI** specification (in the **SPI** decoder 62) or the HT specification (in the HT decoder 64). One of the decoders ...circuit 26A-26C that received the packet. In particular, if the Rx circuit is receiving **SPI**-4 phase 2 traffic, the LE bit may indicate, when set, that a DIP-4 error occurred. The SE bit may indicate, when set, that a **SPI**-4 abort control word was received in the packet or an error was detected in... ...field stores the IVC for a received packet, if the packet was transmitted on the **SPI** interface. For output queue descriptors, the VC field may store a value for which the... ...28C may append the bits to the OVC to generate the VC field in the **SPI**-4 packet. The memory buffer address field stores the address of the memory buffer indicated...

Specification: ...interfaces using the PoHT extension. Alternative, such interfaces 30A-30C may be system packet interfaces (**SPI**) according to any level of the **SPI** specification set forth by the Optical Internetworking Forum (e.g. level 3, level 4, or level 5). In one particular embodiment, the interfaces may be **SPI**-4 phase 2 interfaces. In the illustrated embodiment, each interface circuit 20A-20C may be configurable to communicate on either the **SPI**-4 interface or the HT interface. Each interface circuit 20A-20C may be individually programmable, permitting various combinations of the HT and **SPI**-4 interfaces as interfaces 30A-30C. The programming may be performed in any fashion (e... ...g. transmitting the packet data as a payload of a command, such as PoHT). The **SPI**-4 interface may define 16 hardware virtual channels, extendable to 256 virtual channels in software...example, the interface 306 may be a HT interface (using the PoHT extension) or the **SPI**-4 interface, as desired. As used herein, a packet circuit includes any circuit which sources... ...example, the packet circuit 302 may be a media access control (MAC) circuit having a **SPI**-4 or HT packet interface. The packet circuit 302 may further comprise switches, routers, gateways... ...on the interface 308. In another embodiment, if desired, the interface 308 may be a **SPI**-4 interface if internode coherency is not used in the packet processing system 300.

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System having interfaces and a switch that separates coherent and non-cohrent data packet traffic

System mit Schnittstellen und einem Schalter fur die Trennung von koharentem und nichtkoharentem Datenpaketverkehr

Systeme avec des interfaces et un commutateur pour la separation de trafic coherent et non-coherent de paquets de donnees

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Available Text	Language	Update	Word Count
CLAIMS A	(English)	200321	795
SPEC A	(English)	200321	17923
CLAIMS B	(English)	200513	907
CLAIMS B	(German)	200513	865
CLAIMS B	(French)	200513	994
SPEC B	(English)	200513	17991
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Turning now to Fig. 3, an example of traffic received on two... ...the interface 30A may be an HT interface and the interface 30B may be a **SPI** interface. The traffic on the interfaces 30A-30B are illustrated in time order from right... ...switch 18.

The Rx circuit 26B receives only packet traffic in this example (via the **SPI** interface 30B), and thus transmits packets through the switch 18 to the packet DMA circuit 16. If packets are received in different virtual channels on the **SPI** interface 30B, the order of the packets transmitted to the packet DMA circuit 16 may differ from the order on the **SPI** interface 30B (e.g. the packet P3)) is transmitted before the packet P2)) in this... ...embodiment of Fig. 4, the Rx circuit 26A includes a decoder 60 (which includes a **SPI** decoder 62 and an HT decoder 64 including a PoHT BAR1 register 66), a hash... ...receives the input data from the interface 30A and decodes the data according to the **SPI** specification (in the **SPI** decoder 62) or the HT specification (in the HT decoder 64). One of the decoders ...circuit 26A-26C that received the packet. In particular, if the Rx circuit is receiving **SPI**-4 phase 2 traffic, the LE bit may indicate, when set, that a DIP-4 error occurred. The SE bit may indicate, when set, that a **SPI**-4 abort control word was received in the packet or an error was detected in... ...field stores the IVC for a received packet, if the packet was transmitted on the **SPI** interface. For output queue descriptors, the VC field may store a value for which the... ...28C may append the bits to the OVC to generate the VC field in the **SPI**-4 packet. The memory buffer address field stores the address of the memory buffer indicated...

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Turning now to Fig. 3, an example of traffic received on two... ...the interface 30A may be an HT interface and the interface 30B may be a **SPI** interface. The traffic on the interfaces 30A-30B are illustrated in time order from right... ...switch 18.

The Rx circuit 26B receives only packet traffic in this example (via the **SPI** interface 30B), and thus transmits packets through the switch 18 to the packet DMA circuit 16. If packets are received in different virtual channels on the **SPI** interface 30B, the order of the packets transmitted to the packet DMA circuit 16 may differ from the order on the **SPI** interface 30B (e.g. the packet P3)) is transmitted before the packet P2)) in this... ...embodiment of Fig. 4, the Rx circuit 26A includes a decoder 60 (which includes a **SPI** decoder 62 and an HT decoder 64 including a PoHT BAR1 register 66), a hash... ...receives the input data from the interface 30A and decodes the data according to the **SPI** specification (in the **SPI** decoder 62) or the HT specification (in the HT decoder 64). One of the decoders ...circuit 26A-26C that received the packet. In particular, if the Rx circuit is receiving **SPI**-4 phase 2 traffic, the LE bit may indicate, when set, that a DIP-4 error occurred. The SE bit may indicate, when set, that a **SPI**-4 abort control word was received in the packet or an error was detected in...

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